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DESIGN OF LOGIC BIST USING BIPARTITE LFSR

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ABSTRACT

This paper discusses the design of ASIC (Application Specific Integrated Circuit) for LFSR (Linear feedback shift register) for testing of digital VLSI circuits using BIST technique. In this design an ASIC based programmable LFSR is used as Test Pattern Generators (TPG). Implementation of any design on ASIC is only possible with EDA (Electronic Design automation) tools. In this paper the cadence tool is used to accomplish the task. The simulation and synthesis results are presented. Further analysis of power, logic area usage and timing of controller is done on the synthesis results.

KEYWORDS: LFSR, Logic BIST, ASIC, Verilog HDL, Cadence Tool